Reg. No. | | | | | | | | |

G. VENKATASWAMY NAIDU COLLEGE (AUTONOMOUS), KOVILPATTI – 628 502.

UG DEGREE END SEMESTER EXAMINATIONS - NOVEMBER 2025.

(For those admitted in June 2023 and later)

PROGRAMME AND BRANCH: B.Sc., ELECTRONICS

SEM	CATEGORY	COMPONENT	COURSE CODE	COURSE TITLE
II	CORE-3	PART - III	U23EL202	DIGITAL ELECTRONICS

Date & Session:08.11.2025/AN **Time: 3 hours** **Maximum: 75 Marks**

Course Outcome	Bloom's K-level	Q. No.	**SECTION – A (10 X 1 = 10 Marks)** **Answer ALL Questions.**
CO1	K1	1.	Convert $(25)_{10}$ to Octal number system. a)$(21)_8$ b)$(11)_8$ c) $(31)_8$ d) $(41)_8$
CO1	K2	2.	Convert $(26)_{16}$ to Octal number system. a) $(16)_8$ b) $(36)_8$ c) $(26)_8$ d) $(46)_8$
CO2	K1	3.	Which of the following are called as basic gate? a) NAND & NOT b) EXOR & EXNOR c) NAND & NOR d) AND & OR & NOT
CO2	K2	4.	Which of the following is the correct truth table for a NOR gate? a) 0,1,1,1 b)1,0,0,1 c) 1,1,0,0 d) 0,0,0,1
CO3	K1	5.	A full adder consist of a) 2HA and 1NOT Gate b)2HA and 1ORGate c) 2HA and 1AND Gate d)2HA and 2OR Gate
CO3	K2	6.	What is the number of input taken by 1 bit half adder? a) 1 b)2 c) 3 d) 4
CO4	K1	7.	What is the name of the storage elements used in clocked sequential circuits? a) Latches b) Flip-Flops c) Logic Gates d) All the above
CO4	K2	8.	What happens to output of T Flip-Flop when T=0? a) 0 b)1 c) No change d)Toggle mode
CO5	K1	9.	RAM is also known as _____. a) Read/Write Memory b) PROM c) EAROM d) EPROM
CO5	K2	10.	FPGA stands for _____. a) Field Program Gate Array b) First Program Gate Array c) Field Programmable Gate Array d) First programmable Gate Array
Course Outcome	**Bloom's K-level**	**Q. No.**	**SECTION – B (5 X 5 = 25 Marks)** **Answer ALL Questions choosing either (a) or (b)**
CO1	K3	11a.	Perform the following. $(010\ 1100)_2 = (?)_{10}$, $(1010)_2 = (?)_{10}$ **(OR)**
CO1	K3	11b.	Find the decimal number $(764)_{10}$ into binary number.

CO2	K3	12a.	Explain Demorgan's Theorem. **(OR)**
CO2	K3	12b.	Demonstrate and explain AND & NOR logic gates.
CO3	K4	13a.	Identify the Half adder circuit and explain it with Truth Table. **(OR)**
CO3	K4	13b.	Illustrate the Demultiplexer.
CO4	K4	14a.	Explain JK Flip – Flop **(OR)**
CO4	K4	14b.	Compare Synchronous Counter & Asynchronous Counter.
CO5	K5	15a.	Compare Volatile Memory & Non-Volatile Memory. **(OR)**
CO5	K5	15b.	Justify the concept of Programmable logic Arrays.

Course Outcome	**Bloom's K-level**	**Q. No.**	**SECTION – C (5 X 8 = 40 Marks)** **Answer ALL Questions choosing either (a) or (b)**
CO1	K3	16a.	Find the following Decimal number to hexa, Octal and Binary number. 1) $(8424)_{10}$ 2) $(979)_{10}$ **(OR)**
CO1	K3	16b.	Write short note on 1) ASCII code 2) EBCDIC code
CO2	K4	17a.	Demonstrate and explain Ex – OR, NOR & Ex-NOR logic gates. **(OR)**
CO2	K4	17b.	Simplify the following expression $f(X,Y,Z) = \sum_m (0,2,5,7)$ using K Map
CO3	K4	18a.	Build the Full Subtractor circuit & explain its working with Truth Table **(OR)**
CO3	K4	18b.	Construct 3 to 8 Decoder using logic gates & explain its working with Truth Table
CO4	K5	19a.	Inspect the working of JKMS flip flop with proper diagram. **(OR)**
CO4	K5	19b.	Examine the Serial-In Serial-Out Shift Register
CO5	K5	20a.	Assess the working of ROM. **(OR)**
CO5	K5	20b.	Sketch the diagram of Field Programmable Gate Arrays and explain it.